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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/933,297	08/20/2001	Setho Sing Fee	4738US (00-1113)	5686

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 07/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/933,297	FEE ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *13-35 and 41-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 36-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5-20-4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claims 13-35 and 41-44 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 10-14-3.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-12 and 36-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over McLellan (6498099) and Lin (6700188).

At column 1, lines 22-24; column3, line 9 to column 4, line 47, McLellan discloses the following:

A method of fabricating an integrated circuit package comprising: providing a semiconductor die 206 having a plurality of bonds on an active surface thereof; providing a lead frame 100 including a plurality of conductive leads 203, electrically coupling 205 a first bond of the plurality of bonds to a first portion of at least one conductive lead of the plurality of conductive leads; electrically coupling a second bond of the plurality of bonds to a second portion of the at least one conductive lead; and electrically isolating the first portion of the at least one conductive lead from the second portion of the at least one conductive lead; further comprising encapsulating the semiconductor die and at least a portion of the lead frame in a dielectric material 401; wherein the electrically isolating the first portion from the second portion is effected subsequent to the encapsulating; wherein the electrically isolating the first portion from the second portion of the at least one conductive lead inherently includes mechanically severing the at least one conductive lead between the first portion and the second portion; wherein the electrically isolating the first portion from the second

portion of the at least one conductive lead includes etching to sever the at least one conductive lead between the first portion and the second portion; wherein the electrically coupling the first bond to a first portion of the at least one conductive lead includes wire bonding; wherein the electrically coupling the second bond to the second portion of the at least one conductive lead includes wire bonding; further comprising forming a notched region in a surface of the at least one conductive lead between the first portion and the second portion; further comprising encapsulating the semiconductor die and at least a portion of the lead frame including the notched region of the at least one conductive lead in a dielectric material; wherein the electrically isolating the first portion from the second portion includes separating the first portion from the second portion while leaving at least some dielectric material in the notched region; wherein the separating the first portion from the second portion includes cutting (via etching) the at least one conductive lead into the notched region from an opposing surface of the at least one conductive lead.

A method of forming an array of electrically conductive elements on an integrated circuit package, the method comprising: securing a semiconductor die having a plurality of bonds on an active surface thereof to a lead frame having a plurality of leads; electrically coupling each lead of the

plurality of leads at spaced locations with one of at least two different bonds of the plurality of bonds; and severing each lead between the spaced locations to form at least two electrically isolated conductive elements.

A method of fabricating a semiconductor die assembly, comprising: placing a semiconductor die within a plurality of leads extending laterally outwardly from peripheral edges thereof; wire bonding bonds on the semiconductor die to spaced locations on the leads of the plurality; transfer molding a dielectric encapsulant over the semiconductor die, wire bonds and leads, leaving undersurfaces of the leads exposed; and severing the leads between the spaced locations; further comprising notching upper surfaces of the leads between the spaced locations before the placing the semiconductor die within the plurality of leads; wherein the placing the semiconductor die includes securing the semiconductor die to a die paddle 202 located within the plurality of leads; wherein the severing is effected by making a linear cut (via etching) between the spaced locations on each lead extending from a common peripheral edge; further comprising notching upper surfaces of the leads between the spaced locations before the placing the semiconductor die within the plurality of leads, and wherein the linear cut is extended substantially only to a depth sufficient to intersect bottoms of the notches so that some dielectric encapsulant remains between the spaced locations.

To further clarify the disclosure of inherently mechanically severing, it is noted that the severing inherently uses etching tools; hence the severing inherently relates to tools. In addition, the etching relates to, is governed by, and is done in accordance with the principles of mechanics.

However, McLellan does not appear to explicitly disclose a plurality of bonds pads on an active surface of the die.

Nevertheless, at column 4, lines 57-60, Lin discloses a plurality of bonds pads 210a on an active surface of a die 210. Moreover, it would have been obvious to combine the processes of McLellan and Lin because it would facilitate wire-bonding.

Claims 4 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over McLellan and Lin as applied to claims 1 and 36, and further in combination with McLellan (6372539).

McLellan (6498099) and Lin does not appear to explicitly disclose mechanical severing in the sense of severing caused by, resulting from, or relating to a process that involves a purely physical as opposed to a chemical change, or wherein the severing is effected by making a linear cut between the spaced locations.

Notwithstanding, at column 5, lines 13-15; and column 6, line 60 to column 7, line 9, McLellan (6372539) explicitly discloses mechanical severing

"saw," in the sense of severing caused by, resulting from, or relating to a process that involves a purely physical as opposed to a chemical change, and wherein the severing is effected by making a linear cut between spaced locations "half-etched portion."

Furthermore, it would have been obvious to use or substitute the severing of McLellan (6372539) for at least some of the severing of McLellan (6498099) because it would provide severing, and use and substitution of a known element based on its suitability for its intended use has been held to be prima facie obvious. See MPEP 2144.07. Also, it would have been obvious to substitute the severing of McLellan (6372539) for at least some of the severing of McLellan (6498099) because it would provide alternative severing when the severing of McLellan (6498099) becomes infeasible, e.g., when the severing of McLellan (6498099) is cost ineffective.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Head SAE Linda Hodge-Taylor whose telephone number is 571-272-1585.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
7-Jul-04